Chapter 8

PULSE AND SWITCHING CIRCUITS

SECTION I. SWITCHING CHARACTERISTICS

8–1. General

a. Circuit Applications. Pulse and switching circuits are used in radar, television, telemetering, pulse-code communication, and computer equipments. The circuits operate as relaxation oscillators, amplifiers, inverters, frequency dividers, and wave shapers to perform the functions of limiting, triggering, gating, and signal routing. Some typical circuits are described in this chapter; triggered circuits are covered in Section II and gating circuits are covered in Section III.

b. Nonlinear Operation. Pulse and switching circuits are normally characterized by large-signal, or *nonlinear,* operation of the tunnel diode. These circuits usually require the application of a pulse for operation (par. 8–2). The input trigger pulses produce large and sudden changes in output voltage or output current. Nonlinear operation of this type usually results in output waveforms differing considerably from the input waveforms.

c. Unit Step Voltage. 1. Pulse waveforms widely encountered in large-signal operation of the tunnel diode are illustrated in Fig. 8–1. The *instantaneous* changes in voltage levels represent the *ideal* pulse. The effect of the tunnel diode on the ideal pulse is given in paragraph 8–4.

2. A voltage which experiences an instantaneous change in amplitude from one constant level to another is called a *unit step voltage.* When the unit step voltage is the *applied signal* to a switching circuit, it is usually of sufficient magnitude to cause the circuit output to change from a low-voltage state to a high-voltage state or vice versa.

3. Figure 8–1A shows a *positive* unit step voltage occurring at time $t1$. A positive unit step voltage increases a positive potential level to a higher positive potential level and decreases a negative potential level to a less negative potential level. Depending on the magnitude of the positive unit step voltage, a negative potential level may even be changed to a positive

potential level. Figure 8–1B shows a *negative* unit step voltage occurring at time $t2$. A negative unit step voltage increases a negative potential level to a higher negative potential level and decreases a positive potential level to a less positive potential level or even to a negative potential level. Figure 8–1C shows the formation of an ideal pulse (square or rectangular) by two unit step voltages, one positive (time $t1$) and one negative (time $t2$).

Note: Unit step currents occur in the same manner as unit step voltages. Current levels, rather than voltage levels, undergo instantaneous positive or negative changes.

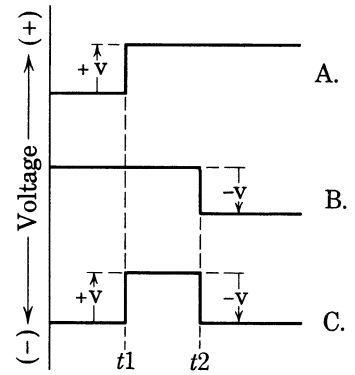


FIG. 8–1. Positive and negative unit step voltages, showing formation of a pulse

8–2. Types of Operation

All pulse and switching circuits are classified as astable, monostable, or bistable. These terms are discussed in detail in paragraph 7–10 as they apply to a single tunnel diode circuit, and in paragraph 7–12 as they apply to a coupled-pair circuit. In addition, astable (free-running) relaxation oscillators are covered in Chapter 7. Monostable and bistable circuits are covered in paragraphs 8–5 through 8–9. The outstanding aspect of each circuit is as follows:

a. The astable circuit requires only the application of dc power for operation. The values of the circuit elements will determine the rate at which the circuit will switch from a high-voltage level to a low-voltage level and vice versa. Trigger input pulses may be introduced into the circuit *only to synchronize the output of the circuit with another signal.*

b. The monostable circuit requires dc power for operation as well as an input trigger pulse to switch it from its normally stable condition in the high- or low-voltage state (positive-resistance regions). After the trigger pulse *initiates* the change in the state of the circuit, the circuit will of its own power switch to the nonstable state and then return to its single stable condition. The time required for each complete action depends upon the values of the circuit elements. The action is repeated for each input pulse.

c. The bistable circuit requires dc power as well as *two* input trigger pulses for a *complete* switching action. Depending on its previous history, the bistable circuit may be found at rest in either the low-voltage or the high-voltage state. One trigger pulse will initiate action to switch the circuit from the state in which it is *found* to the other state; a *second* trigger

pulse is required to initiate action to switch the circuit to its original state. The speed with which the circuit switches from one state to another depends primarily on the parameters of the particular tunnel diode used (par. 8–4).

8–3. On and Off States

The terms *on* and *off*, when used to describe electron tubes or transistors operating as switches, are for the most part self-explanatory. The term *on* with respect to these devices refers to heavy (usually saturation) current flow and low voltage between cathode and plate or emitter and collector, respectively. The term *off* refers to zero (or very low) current flow and high voltage between cathode and plate or emitter and collector. In the case of the tunnel diode (Fig. 8–2) the term *off* means that the tunnel diode is in the high-voltage state (biased beyond the valley-current point); the term *on* means that the tunnel diode is in the low-voltage state (biased below the peak-current point). In a particular application as a switch the tunnel diode current in the *off* or the *on* state may very well be the same magnitude; therefore these terms do not necessarily imply differences in *current* flow. The terms are arbitrarily chosen and used to mean just the opposite in some of the literature. The terms *on* and *off* as defined here, however, with respect to the tunnel diode keep the same *voltage* output condition consistent for all three devices (electron tube, transistor, and diode); i.e., *on* indicates low voltage and *off* indicates high voltage across the particular device.

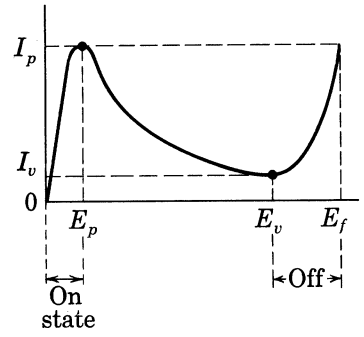


FIG. 8–2. Tunnel diode showing *on* and *off* switching regions

8–4. Tunnel Diode Switching Speed

a. The speed with which the average tunnel diode switches from the *on* to the *off* state or vice versa is very high. Some practical diodes switch in less than one nanosecond (mμs). The speed is determined mainly by the diode junction capacitance and the magnitude of the trigger pulse current. A current pulse which momentarily raises the diode current to a value larger than the peak current (Fig. 8–2) will switch the diode from the *on* state to the *off* state. A current pulse which momentarily lowers the diode current to a value less than the valley current will switch the diode from the *off* state to the *on* state. A measure of the switching speed is referred to as the *tunnel diode voltage rise time.* The rise time indicates the time

required for the pulsed tunnel diode voltage to climb from 10% of its maximum value to 90% of its maximum value. The formula used to calculate the rise time is as follows:

$$t_r = \frac{(E_f - E_p)C_D}{(I_p - I_v)10^3}$$

wherein:

t_r = rise time in nanoseconds

E_f = tunnel diode forward injection voltage in mv

E_p = peak-current voltage in mv

C_D = junction capacitance in $\mu\mu$f

I_p = peak current in ma

I_v = valley current in ma

This formula is based on a tunnel diode fed from a constant-current load line and triggered by a pulse having a minimum amplitude. An example of the use of this formula is given in *b* below.

b. Assume that it is desired to find the rise time of a tunnel diode having the following values:

E_f = 500 mv

E_p = 70 mv

C_D = 40 $\mu\mu$f

I_p = 10 ma

I_v = 1 ma

Substitute these values in the formula for rise time (*a* above):

$$t_r = \frac{(500 - 70)40}{(10 - 1)10^3}$$

$$= \frac{17{,}200}{9 \times 10^3}$$

Therefore, t_r = 1.9 nanoseconds.

Note: The values required to calculate t_r for a given tunnel diode are normally given in the manufacturer's specifications for the tunnel diode.

SECTION II. TRIGGERED CIRCUITS

8–5. Monostable Multivibrator, Single Diode

Figure 8–3A shows a monostable multivibrator, also referred to as a one-shot, single-shot, or single-swing multivibrator. The circuit is biased in the stable *on* region (*a* below) or the stable *off* region (*b* below). A single pulse causes the circuit to switch from its biased stable region to the other stable region and of its own accord returns to its biased stable region. The energy stored in the field of coil $L1$ furnishes the power required to switch the diode. Resistor $R1$ is the diode load resistor and its value in conjunction with the value of bias voltage (E_B) determines the stable region at quiescence. Capacitor $C1$ and resistors $R2$ and $R3$ form the pulse input network. Capacitor $C1$ is a blocking capacitor, resistor $R3$ is a dc return resistor, and resistor $R2$ is an isolating resistor that prevents loading of the pulse source by the tunnel diode.

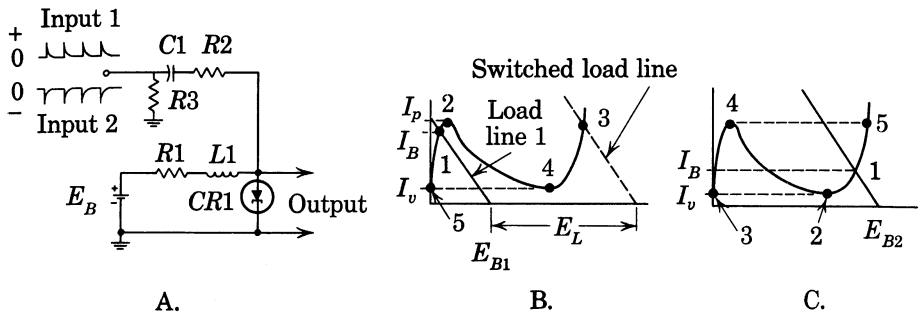


FIG. 8–3. Monostable multivibrator biased in the *on* or the *off* region

a. On Region. Figure 8–3B shows the relation of the diode characteristic and the load line with a given bias voltage (E_{B1}). At quiescence the circuit is stable at point 1 and current I_B flows through resistor $R1$, coil $L1$, and diode $CR1$. Assume that a positive-going input pulse (input 1) of current equal in magnitude to $I_p - I_B$ is introduced through capacitor $C1$. The operating point rises to point 2, peak current. At this point when the current through the diode would normally fall (negative resistance), the field about coil $L1$ starts to collapse and switches the operating point almost instantaneously to point 3, also a stable point. Note that the action of coil $L1$ is to create a voltage (E_L) which adds to bias voltage E_{B1} and causes the load line to move to the right and intercept the diode curve at point 3; note also the switched load line. From point 3 to point 4 the field of coil $L1$ continues to discharge relatively slowly and voltage E_L is diminishing in magnitude. At point 4 (the valley current) the circuit again reaches the negative-resistance (unstable) region where the current would tend to rise. The action of the coil is to keep the current constant and the circuit switches almost instantaneously to point 5. During this period the voltage across the coil opposes bias voltage E_{B1}. The circuit then returns relatively slowly to point 1, the biased stable condition. From point 5 to point 1 the opposing voltage of the coil diminishes to zero. The resultant output is one rectangular wave. Another positive-going pulse will cause the cycle to repeat.

b. Off Region. The same-valued circuit elements can be used to bias the multivibrator in the *off* region (Fig. 8–3C); only the bias voltage need be increased to that shown (E_{B2}). The circuit is now stable at quiescent point 1. A *negative*-going input pulse (input 2) is now required to switch the circuit through one complete cycle. The pulse magnitude must equal $I_B - I_v$. An action similar to that described in *a* above occurs with the circuit switching rapidly from point 2 to point 3, going relatively slowly from point 3 to point 4, rapidly from point 4 to point 5, and slowly from point 5 to point 1 to complete a cycle. The action will repeat with each negative-going pulse.

8–6. Bistable Multivibrator, Single Diode

a. The basic bistable single diode multivibrator is shown in Fig. 8–4A. It consists of a bias supply (E_B), a load resistor ($R1$), and a tunnel diode ($CR1$); capacitor $C1$ is used only to couple a trigger pulse into the circuit. An alternate method of introducing the trigger pulse is shown in Fig. 8–4B. Coil $L1$ has been added only to prevent shunting of the input pulse to ground by the bias battery. Note that the bistable circuit does *not* require an energy-storing element (an inductance) for operation, as in the case of the astable and monostable circuits. The discussion in *b* below applies to either circuit (Fig. 8–4A or B).

b. Figure 8–4C shows that the load line ($R1$) intersects the diode curve in two stable points, 1 and 2; the intersection in the negative-conductance region, of course, is unstable. A positive-going input pulse ($+E_p$) raises the current in the diode to the peak value, effectively increases the bias voltage ($E_B + E_p$), and causes the load line to rise so that it intersects the curve at 1′ and 2′. The diode switches almost instantaneously to point 2′; with the passing of the trigger pulse, the circuit comes to rest at point 2. Note that in going from point 1 to point 2 there has simply been a different division of the bias voltage (E_B); in the *on* state there was a small portion of the bias voltage across the diode and a high portion across the resistor; in the *off* state this condition is reversed. A negative-going input pulse ($-E_p$) lowers the current through the diode to the valley current, effectively lowers the bias voltage ($E_B - E_p$), and causes the load line to fall so that

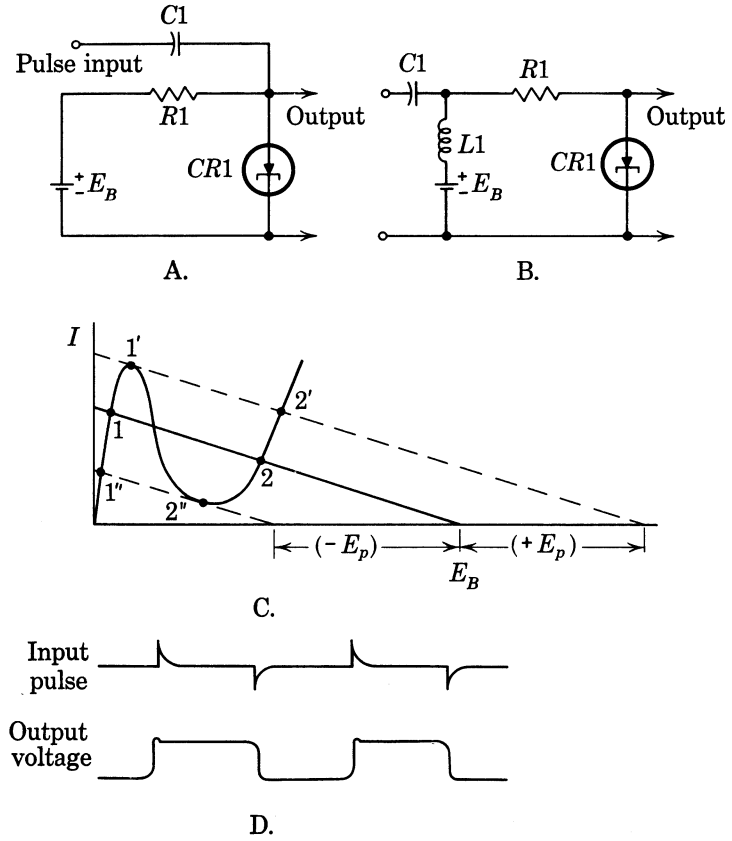


FIG. 8–4. Basic bistable circuit, showing alternate methods of triggering, load line on diode curve, and input pulses and output waveform

it intersects the diode curve at 1″ and 2″. The diode switches almost instantaneously to point 1″; with the passing of the trigger pulse the diode comes to rest at point 1. The relationship between the input pulses and the output waveform are shown in Fig. 8–4D.

Note: If a negative input pulse is introduced when the circuit is in the *on* state (point 1), the load line is temporarily lowered and then returns to point 1 with no switching occurring. If a positive pulse is introduced when the circuit is in the *off* state (point 2), the load line is temporarily raised, but no switching occurs.

8–7. Bistable Multivibrator, Increased Sensitivity

A very sensitive bistable multivibrator can be made by using a tunnel diode and a rectifying diode (*a* below), or by using a tunnel diode and a

transistor (*b* below). As used here, the sensitivity of a bistable multivibrator refers to the magnitude of the trigger pulses required to initiate switching action. The smaller the required pulse magnitude, the more sensitive the circuit.

a. Tunnel Diode and Rectifying Diode. High sensitivity can be obtained with the basic bistable multivibrator (Fig. 8–4A) by selecting a load resistor and a bias voltage so that the load line intersects the *on* region of the diode curve close to the peak current, and also intersects the *off* region of the diode curve close to the valley current. Such a load line is shown intersecting points 1 and 3 in Fig. 8–5B. Low-valued positive and negative trigger pulse currents would initiate switching resulting in high sensitivity. However, because of the difference in the slopes of the diode curves in the *on* and *off* regions, a nonsymmetrical output will result. The resistance in the positive region is higher than that in the *on* region. A circuit used to overcome this difficulty and still retain high sensitivity is shown in Fig. 8–5A. The battery, resistor $R2$, and tunnel diode $CR1$ form the basic bistable multivibrator (par. 8–6). Isolating resistor $R1$ prevents loading of the pulse source by the tunnel diode. To the basic circuit has been added a

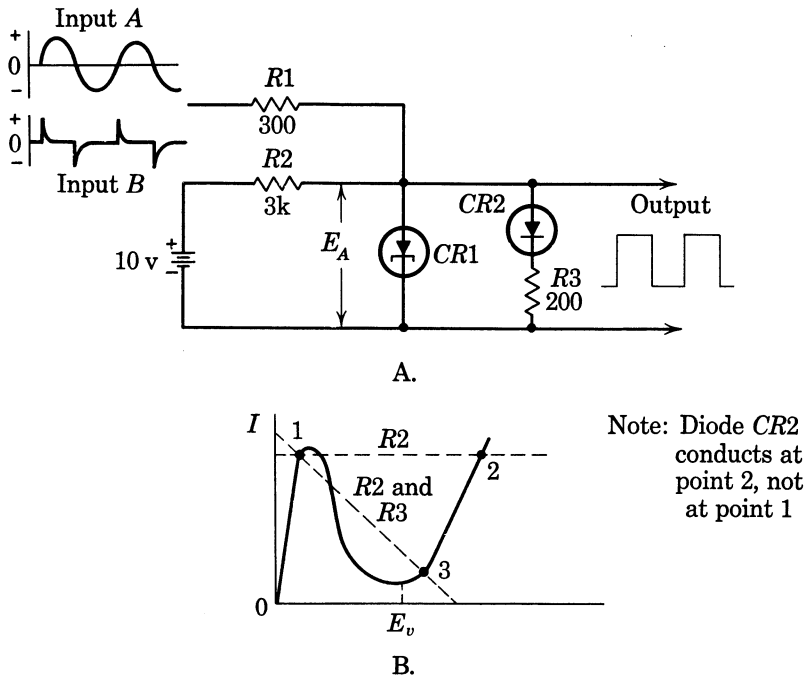


FIG. 8–5. High sensitivity bistable multivibrator showing biasing technique

normal rectifying diode ($CR2$) and resistor $R3$. The normal rectifying diode, unlike the tunnel diode, does not start conducting when forward biased until the voltage is approximately equal to the tunnel diode valley voltage (E_v), and then it conducts heavily. Figure 8–5B shows the load line for resistor $R2$ and indicates that in the *on* state the circuit is biased at point 1; diode $CR2$ is nonconducting. A small, positive-going input pulse would switch the circuit rapidly to point 2. At point 2 diode $CR2$ conducts and effectively places low-valued resistor $R3$ in parallel with the tunnel diode. The effective load line composed of resistors $R2$ and $R3$ causes

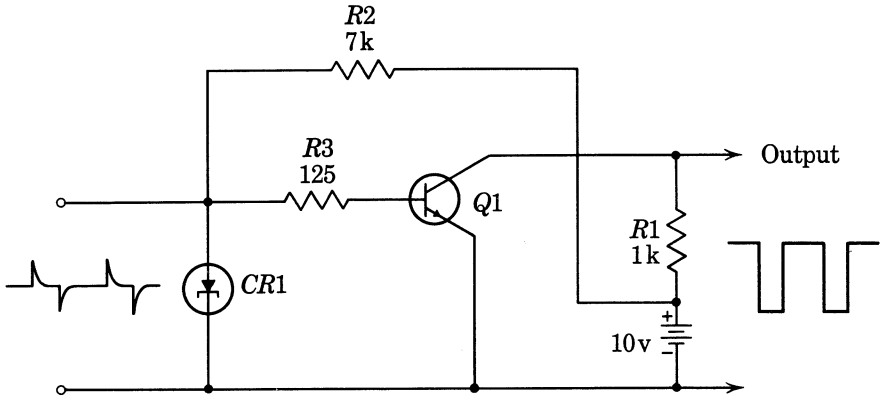


FIG. 8–6. Bistable multivibrator using tunnel diode and transistor

the circuit to be biased at point 3 in the *off* state. Because of the low resistance, the circuit falls rapidly from point 2 to point 3. A negative-going input pulse will switch the circuit rapidly from 3 to 1, causing diode $CR2$ to become nonconducting and setting the circuit for another cycle. The input to this circuit could be a sinewave (input A) or pulses (input B). If a sinewave is used, the circuit is referred to as a *squarer*.

b. Tunnel Diode and Transistor. A very sensitive bistable multivibrator using a tunnel diode ($CR1$) and an n-p-n transistor ($Q1$) is shown in Fig. 8–6. The main difference between this circuit and that shown in Fig. 8–5A is that rectifying diode $CR2$ has been replaced by the base-emitter junction of transistor $Q1$. When the tunnel diode is in the *on* state, resistor $R2$ biases the diode close to the peak current; the base-emitter junction of the transistor is nonconducting. When the tunnel diode is in the *off* state, the base-emitter junction conducts and parallels the tunnel diode with low-valued resistor $R3$ so that the circuit is biased close to the valley-current point of the tunnel diode. Resistor $R1$ acts as the collector load for transistor $Q1$. With the tunnel diode in the *on* state, the transistor is cut off and its

collector voltage is high (almost equal to the battery voltage). A small positive input pulse rapidly switches the tunnel diode to the *off* state; transistor $Q1$ conducts and saturates; collector voltage drops to near zero. A small negative input pulse rapidly switches the tunnel diode to the *on* state; transistor $Q1$ cuts off and its collector voltage rises to the battery voltage. The cycle is repeated with each pair of positive and negative pulses.

Note: If a p-n-p transistor is used, the battery and the tunnel diode must be reversed in their respective positions. A negative pulse will then switch the tunnel diode from the *on* to the *off* state; a positive pulse will switch the tunnel diode from the *off* to the *on* state.

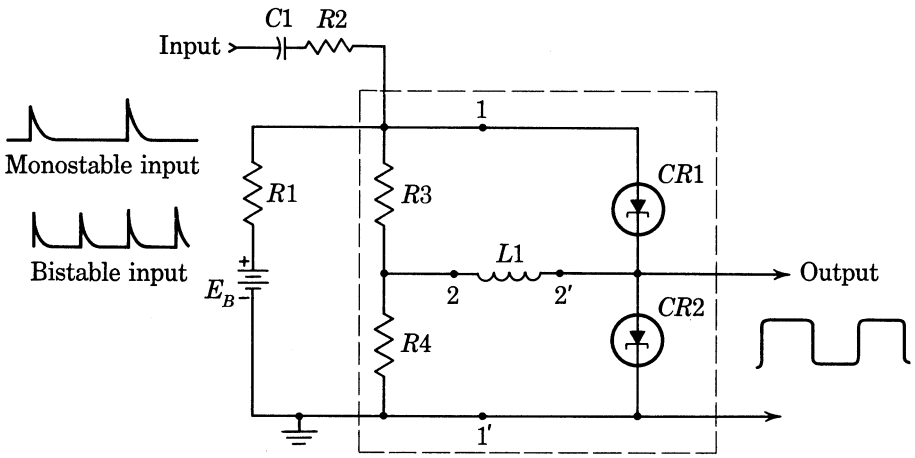


FIG. 8–7. Monostable or bistable coupled-pair multivibrator

8–8. Monostable or Bistable Multivibrator, Coupled Pair

The basic coupled-pair tunnel diode circuit is shown in dashed lines in Fig. 8–7A. The development of a family of characteristic curves for this *device* is covered in paragraph 6–7. An astable multivibrator using the coupled pair is covered in paragraphs 7–12 and 7–13. A monostable multivibrator is covered in *a* below; a bistable multivibrator is covered in *b* below. In the circuit shown, resistors $R1$, $R3$, and $R4$ form a voltage divider and establish the quiescent bias voltage for diodes $CR1$ and $CR2$. Capacitor $C1$ is a blocking capacitor and couples the trigger pulses into the circuit. Isolating resistor $R2$ prevents loading of the pulse source. Coil $L1$ is the energy-storing element required for switching action.

a. Monostable Circuit. For monostable operation, it is required that the values of resistors $R1$, $R3$, and $R4$ be so chosen that their combined *effective* resistance (actually in series with coil $L1$) results in a load line that inter-

sects the diode-pair curve at one point in a positive-resistance region. To accomplish this, resistors $R3$ and $R4$ must be different in value. Depending on the choice of values, load line 1 (Fig. 8–8A) may be chosen, or load line 2; in each case monostable operation will result. If load line 1 or

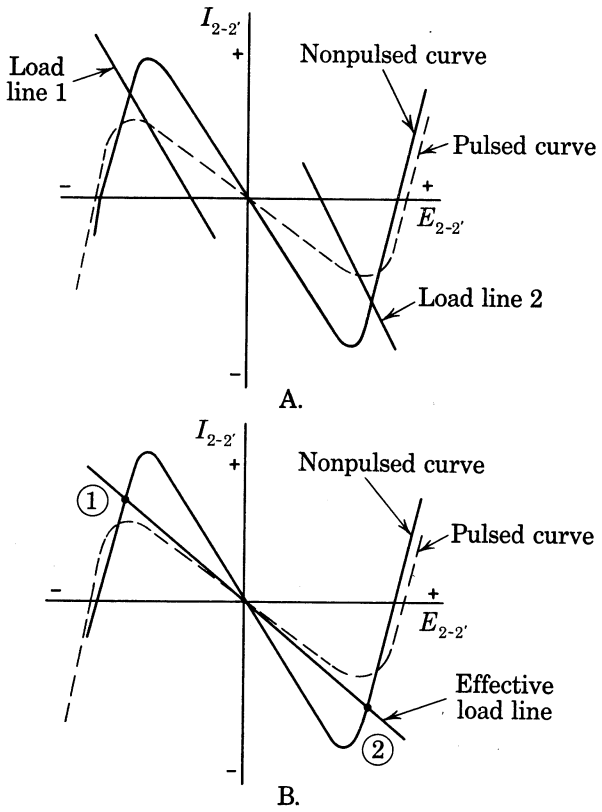


FIG. 8–8. Relationships of load lines and coupled-pair characteristic for monostable and bistable operation

load line 2 is used, the same *positive* trigger pulse will initiate switching action. The trigger pulse momentarily changes the input bias voltage and the diode-pair curve to that shown in dashed lines. This change causes the load line (either 1 or 2) to fall in the negative-resistance (unstable) region and rapid switching occurs. The load line moves to the opposite stable region and back to the *original* stable bias region to complete one cycle. This action occurs for each positive input pulse. Because the positive-resistance regions of the diode-pair curve are symmetrical, a symmetrical

output wave results. Note that the same action would occur if the trigger pulse were introduced in series with battery E_B.

b. Bistable Circuit. For bistable operation it is required that the load line intersect the diode-pair curve in each positive-resistance region (Fig. 8–8B). Such a load line will result if resistors $R3$ and $R4$ (Fig. 8–7) are equal in value and of the proper magnitude. A positive trigger pulse momentarily changes the input bias voltage and the diode-pair curve to that shown in dashed lines. This change causes the load line to fall into the negative-resistance (unstable) region and switching occurs. If the circuit was at rest at point 1, it will now come to rest at point 2; if it was at rest at point 2, it will now come to rest at point 1. Note that a *positive* input pulse can switch the circuit in *either* direction. A second positive trigger pulse will complete one cycle. In addition to having a *symmetrical* output waveform, the coupled-pair bistable multivibrator has a second advantage over the single tunnel diode bistable multivibrator (par. 8–6) in that triggering pulses of only *one polarity* are required by the coupled pair.

8–9. Controlled-Negative-Resistance Multivibrator

a. A two-tunnel diode controlled-negative-resistance *device* is shown in dashed lines in Fig. 8–9A. A discussion of the development of the family of characteristics for this device is given in paragraph 6–8. The most important property of this circuit is the variation in negative resistance at terminals 2–2′ in accordance with the control current introduced at terminals 1–1′ (Fig. 8–9B). This feature permits the construction of a multivibrator with an output waveform, the amplitude of which can be controlled. The circuit shown is a monostable multivibrator. The basic multivibrator is formed by load resistor $R3$, the energy-storing element (coil $L1$), and bias battery E_B in conjunction with the negative resistance displayed at terminals 2–2′. The values of load resistor $R3$ and battery voltage E_B are selected so that the circuit is stable only at one point in the *on* region of the *device*. Capacitor $C2$ couples the trigger pulses to the multivibrator. Resistor $R2$ is large in value and, with battery E_c, produces a constant-current source for biasing the input port. (Actually this bias selects the particular curve of the family of characteristics at which the device will operate at quiescence.) Capacitor $C1$ couples an input signal to the circuit to vary the control current as desired. Note that a step-voltage (staircase) signal is used here.

b. Each input trigger pulse causes the load line to rise above the peak current of the device and enter the unstable region; the circuit switches rapidly to the *off* state. In the *off* state the load line can intercept any of the device curves, depending upon the control current present at that instant.

After a period depending upon the values of resistor $R3$, and coil $L1$, and the resistance of the device in the *off* region, the circuit switches rapidly to its original bias point and completes one cycle. Each trigger pulse will repeat the cycle. As indicated in Fig. 8–9A the trigger pulses and the con-

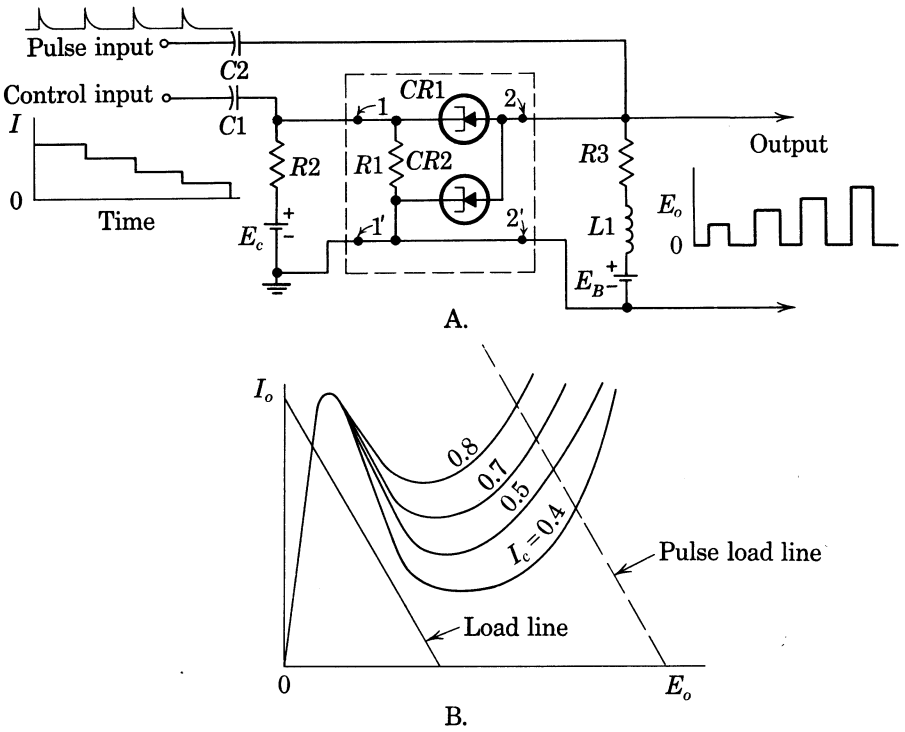


FIG. 8–9. Variable output monostable multivibrator showing relationship of load line and characteristic curves

trol current input signal are synchronized to produce the varying amplitude output.

c. The monostable multivibrator can also be biased in the *off* region of the *device*. In that case a negative trigger pulse would be required for switching. The negative trigger pulse would have to vary in magnitude as required by the control current input signal, or a large enough value would have to be used to ensure switching at any level of control current.

d. With proper biasing this circuit could also be used for astable or bistable operation. In addition, the three tunnel diode controlled-negative-resistance *device* could be used (par. 6–9).

8–10. Pulse Frequency Divider and Staircase Wave Generator

a. The circuit shown in Fig. 8–10 can be used as a pulse frequency divider or a staircase wave generator; these functions are performed simultaneously. In the circuit shown four tunnel diodes are connected in series. This number of diodes will produce a four-step staircase wave (not counting the step at quiescence) for each four input trigger pulses. After the fourth step the output returns to its original voltage level. In addition, the *fourth* input

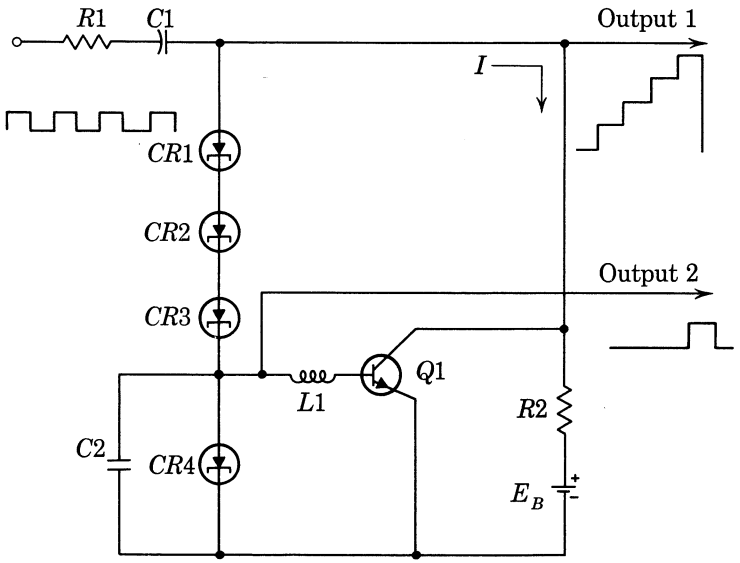


FIG. 8–10. Four-to-one pulse frequency divider and staircase wave generator

trigger pulse produces a pulse output across diode $CR4$, thus providing a four-to-one pulse frequency divider. A larger or a smaller number of diodes can be used; the number of steps of the staircase wave and the pulse frequency division ratio will correspond to the number of diodes used.

b. The development of the combined characteristic curve of series-connected tunnel diodes to form a multistate switch is covered in paragraph 6–5. Diode $CR1$ has the lowest peak current; each diode has a slightly higher peak current than the lower-numbered diode. Diode $CR4$, having the highest peak current, will switch last. Inasmuch as resistor $R2$ and battery E_B form a constant-current source that limits the voltage under quiescent conditions, all the diodes are initially in the *on* state. With diode $CR4$ in the *on* (low-voltage) state, transistor $Q1$ does not conduct. Resistor $R2$ also acts as the transistor collector load. Resistor $R1$ prevents loading of

the pulse source by the tunnel diode circuit. Capacitor $C1$ couples the trigger pulses into the circuit.

c. The first input pulse switches diode $CR1$ to the *off* state and raises the output voltage level by one step. The second, third, and fourth pulses switch diodes $CR2$, $CR3$, and $CR4$, respectively, to the *off* state; with each switching action the output voltage level is increased by one step. Immediately after diode $CR4$ switches, transistor $Q1$ conducts and saturates; its collector voltage drops to near zero and causes all the diodes to *reset* to the *on* state. This action in turn cuts off transistor $Q1$ collector current. A second set of pulses will repeat the cycle. Coil $L1$ and capacitor $C2$ isolate diode $CR4$ from the base-emitter circuit of transistor $Q1$. The time factor introduced by the two elements permits diode $CR4$ to switch to the *off* state before transistor $Q1$ conducts. Switching speed is thereby increased and efficient use is made of the trigger pulse input current.

d. The speed of the circuit is limited by the speed of the reset transistor. The rise time of the staircase wave depends upon the rise time of the trigger pulses. Note that operation of the circuit does not require trigger pulses equally spaced in time.

SECTION III. GATING CIRCUITS

8–11. General

Gating circuits are used most extensively in computers and computer-type equipment. The gating circuits discussed in this section are multiple input bistable tunnel diode circuits which will switch from one stable state to another stable state (produce an output) when certain conditions are met by the input signals. The input signals are most often pulses, or unit step voltages and currents. The conditions to be met by the input signals are usually implied by the designation assigned to a particular type gate.

a. The AND gate, also known as the COINCIDENCE gate, produces an output only if all the input terminals receive input signal pulses simultaneously (par. 8–12, 8–14, 8–15, 8–16, 8–17, and 8–21).

b. The NOT AND gate input requirements are the same as those for the AND gate (*a* above) except that the resultant output is opposite in polarity to the input signal pulses (par. 8–13). The NOT refers to phase inversion.

c. The OR gate produces an output if any one input is present *or* if all inputs are present simultaneously (par. 8–12, 8–14, 8–15, 8–17, and 8–21).

d. The NOR gate is identical with the OR gate except that phase inversion occurs (par. 8–13).

e. The NOT gate is actually a phase inverter (par. 8–18). Unlike the other gating circuits, multiple input signals are not required. A positive

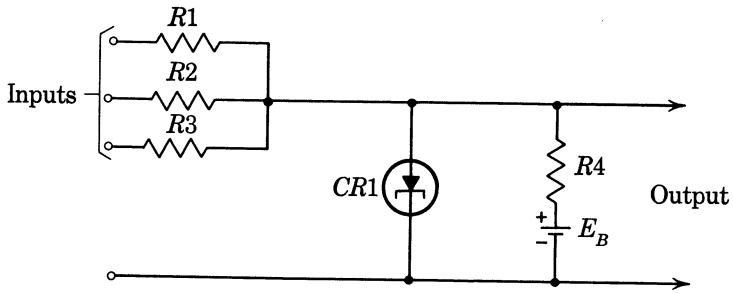
unit step or a negative unit step input voltage results in a negative unit step or a positive unit step output voltage, respectively.

f. The EXCLUSIVE OR gate (par. 8–18) produces a high-level output if one input signal is high, and it will produce a low-level output if both input signals are high.

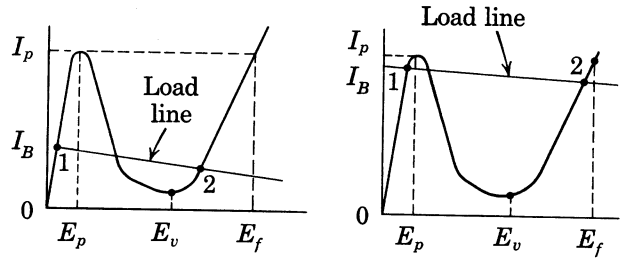
g. The MAJORITY gate (par. 8–19 and 8–20) has an *odd* number of input terminals. The polarity or magnitude of the output signal depends upon the predominant polarity of the input signals. Assume that *three* input pulses are present. If the three are not alike in polarity, the output polarity or magnitude is determined by the two pulses that are alike.

8–12. Biasing for AND or OR Gate

Figure 8–11A shows a basic bistable circuit with multiple inputs. Depending on the bias conditions established, the circuit can operate as an AND gate (*a* below) or an OR gate (*b* below). Resistors $R1$, $R2$, and $R3$ isolate the input pulse sources from each other and prevent loading of the pulse sources by the tunnel diode circuit. Resistor $R4$, in conjunction with bias battery E_B, determines the bistable operating points on the diode characteristic.



A. Basic *AND* or *OR* circuit



B. *AND* biasing C. *OR* biasing

FIG. 8–11. AND or OR gate and biasing condition for each

a. AND Gate. Figure 8–11B shows the normal bias conditions for AND gate operation. Resistor $R4$ load line intersects the diode curve at *a very low point in the on region.* Initially the current through the diode at point 1 equals I_B. The total current input of the pulses required for switching to the *off* state (point 2) must be at least equal to $I_p - I_B$. AND gate operation is assured if all the input pulses are so restricted in magnitude that *all* must be present simultaneously to cause a current increase equal to $I_p - I_B$ to flow through the diode. When this condition is met, the circuit will switch to point 2, another stable point. To perform the AND function again, the circuit must be switched back to point 1. This condition can be achieved by reducing the bias voltage to zero, changing the bias resistor ($R1$) value, or introducing a negative pulse sufficient in magnitude to drive the circuit to the valley-current point causing switching to occur. The latter method is most often used. The pulse used to accomplish this action is referred to as a reset or clearing pulse.

b. OR Gate. Figure 8–11C shows the normal bias conditions for OR gate operation. Resistor $R4$ intersects the diode curve at a point close to the peak current in the *on* region. Initially the current through the diode equals I_B. Switching occurs if the current increase in the diode equals $I_p - I_B$. OR gate operation is assured if each input pulse signal causes a current increase equal to $I_p - I_B$ to flow through the diode. When this condition is met, the diode will switch to point 2 when one or more of the prescribed inputs are present. To repeat the OR function, a negative input reset pulse is required.

8–13. NOT AND or NOR Gate

Biasing techniques for the NOT AND or the NOR gate are identical with those for the AND or the OR gate, respectively (par. 8–11). Figure 8–12 shows a circuit that can be used for a NOT AND or a NOR gate. Circuit

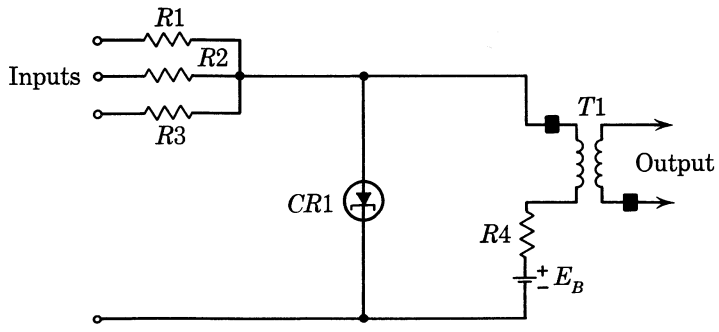


FIG. 8–12. NOT AND or NOR gate

elements in this circuit perform the same function as the correspondingly referenced circuit elements in Fig. 8–11 and have the same values for the corresponding circuit application. In Fig. 8–12, however, transformer $T1$ has been added to provide the negation feature, which is a phase-inversion at the output. In this manner an AND gate is transformed to a NOT AND gate, and an OR gate is transformed to a NOR gate.

8–14. Unidirectional AND or OR Gate

A circuit which can be used as an AND or an OR gate is shown in Fig. 8–13. The basic bistable circuit is inclosed in dashed lines and consists of load resistor $R5$, bias battery E_{B2}, and tunnel diode $CR5$. The circuit is fed from three previous stages through terminals 1, 2, and 3. One preceding stage (tunnel diode $CR1$, load resistor R_1, and bias battery E_{B1}) is shown. Resistors $R2$, $R3$, and $R4$ prevent loading of the input stages by diode $CR5$. *Backward* diodes $CR2$, $CR3$, and $CR4$ ensure unidirectional (left-to-right) flow of energy from the input stage to that in dashed lines. The stage under consideration feeds three succeeding stages connected to terminals 4, 5, and 6. One output stage (load resistor $R9$, tunnel diode $CR9$, and bias battery E_{B3}) is shown. Resistors $R6$, $R7$, and $R8$ prevent loading of diode $CR5$ by the succeeding stages. *Backward* diodes $CR6$, $CR7$, and $CR8$ ensure unidirectional (left-to-right) flow of energy from diode $CR5$ to the succeeding stages. Backward diodes (par. 6–2) must be used for the indicated purpose because the tunnel diode is a one-port, bidirectional device that uses the same two terminals for input and output. The operation of the backward diodes in performing their function is discussed below. Analysis of the circuit as an AND or OR gate is discussed in paragraph 8–15.

a. A comparison of a tunnel diode current-voltage curve and a backward diode current-voltage curve is made in Fig. 8–14A. When the tunnel diode goes through its peak current and valley current, negligible current (considered *leakage* current) flows through the backward diode (although it is forward biased). With reverse bias (less in *magnitude* than the tunnel diode peak voltage) the backward diode conducts very heavily. Because of this the backward diode can be used as a *rectifying* device in the necessarily *low-voltage* circuits of tunnel diodes. The high-voltage requirements of the normal (lightly doped) rectifying diode precludes its use in simple tunnel diode circuits. A comparison of the current-voltage curves of the backward diode and the normal rectifying diode is made in Fig. 8–14B. Note that the backward-diode curve has been reversed and inverted for comparison purposes. When *reverse biased,* the backward diode displays low resistance, whereas the normal rectifying diode displays low resistance when *forward biased* beyond the valley-voltage point of a tunnel diode made of the same material.

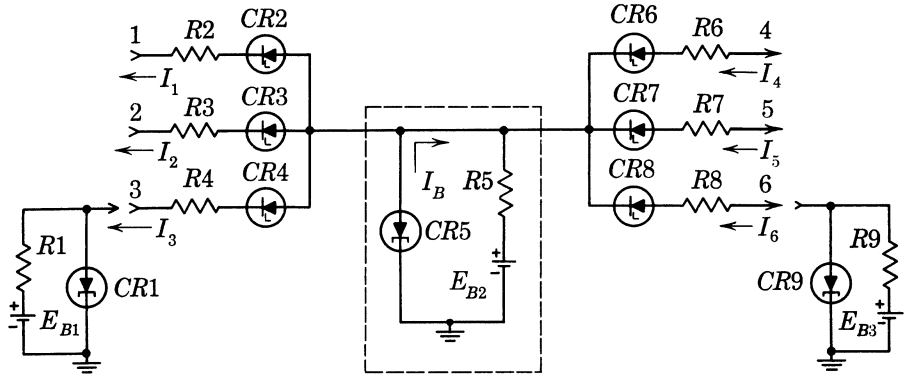


FIG. 8–13. AND or OR gate with multiple input and output terminals

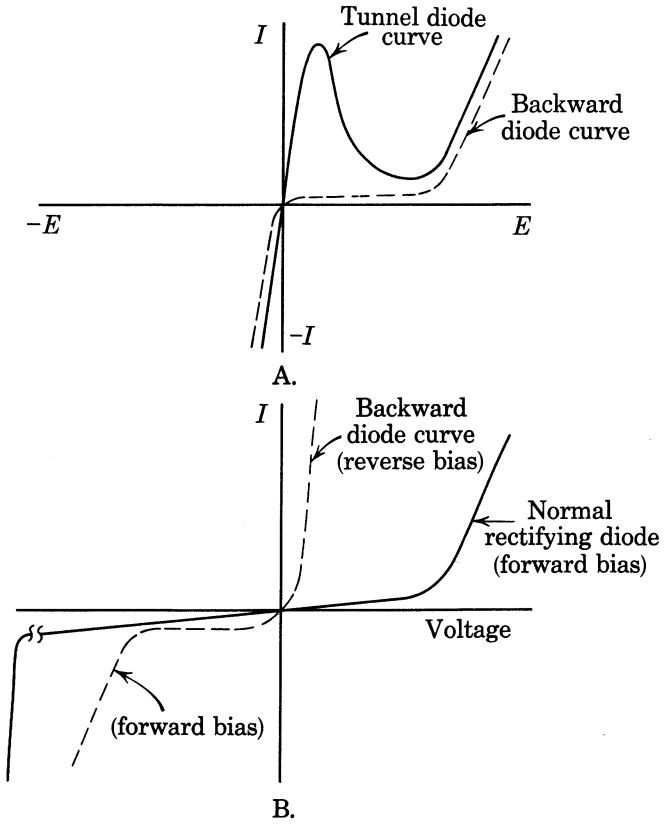


FIG. 8–14. Comparison of tunnel diode and normal rectifying diode current-voltage curves with backward diode current-voltage curve

b. The method by which the backward diode ensures unidirectional energy flow in the gate circuit (Fig. 8–13) is by acting as a rectifier within low-voltage ranges.

1. Figure 8–15A shows a partial schematic of the gate circuit. The input tunnel diode (*CR*1), one isolating resistor (*R*4), one backward diode (*CR*4), and the gate diode (*CR*5) are shown. When input diode *CR*1 is in the low-voltage state and gate diode *CR*5 is in the high-voltage state, backward diode *CR*4 is forward biased in the leakage current region which is a high-resistance region; this point of bias is marked by a dot on the current-voltage curve. The direction of electron flow representing the negligible leakage current is shown by a dashed-line arrow. The backward diode acts on an *open* switch and no energy flows right to left (from diode *CR*5 to diode *CR*1).

2. With the voltage conditions reversed for diodes *CR*1 and *CR*5 (Fig. 8–15B), backward diode *CR*4 is reverse biased (indicated by a dot on the current-voltage curve), and conducts heavily; it acts as a low-resistance or short circuit. The direction of electron-current flow is shown by the arrow. With diode *CR*1 at a higher voltage than diode *CR*5, *energy* flows from left to right, which is desirable.

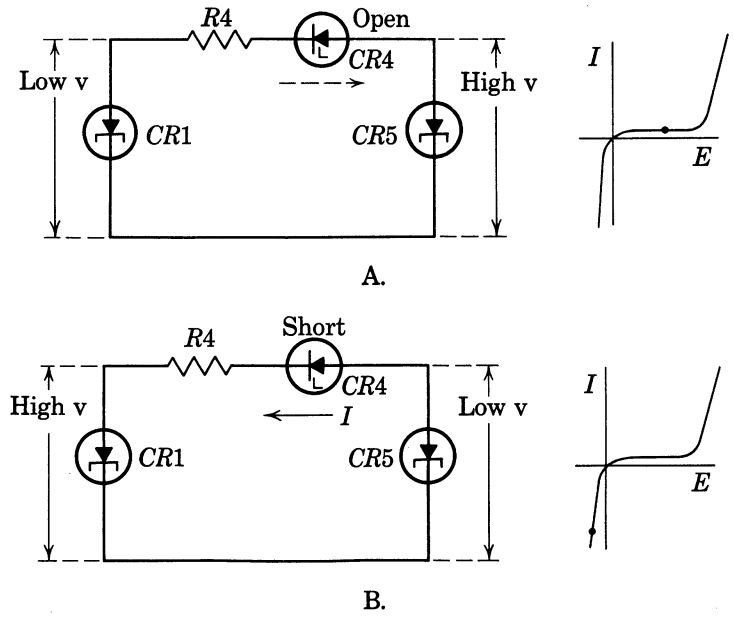


FIG. 8–15. Partial schematic, input and gate diodes, showing effect of different voltage states on backward diode

3. When diodes *CR*1 and *CR*5 are both in the high-voltage state or both in the low-voltage state, zero voltage occurs across backward diode *CR*4; there is no exchange of energy in either direction.

c. Figure 8–16A shows a partial schematic of the gate circuit. The gate diode (*CR*5), one backward diode (*CR*8), one isolating resistor (*R*8), and one output tunnel diode (*CR*9) are shown. With diode *CR*5 in the low-voltage state and diode *CR*9 in the high-voltage state, backward diode *CR*8 is forward biased in the leakage current region (marked by a dot) and acts as an open circuit. There is no flow of energy from right to left. With diode *CR*5 in the high-voltage state and diode *CR*9 in the low-voltage state, diode *CR*8 is reverse biased in the high-current region (marked by a dot); electron current flows in the direction shown by the arrow. Electrical *energy* flows from the high voltage to the low voltage (left to right). When diodes *CR*5 and *CR*9 are in the same voltage state, zero bias occurs across diode *CR*8 and no current or energy flows in either direction.

d. The backward diodes (*CR*2, *CR*3, and *CR*4, Fig. 8–13) also prevent interaction between any two input circuits that may be in different voltage states. Between any two terminals one of the two diodes in series between the terminals will be biased in the leakage current (high-resistance) region

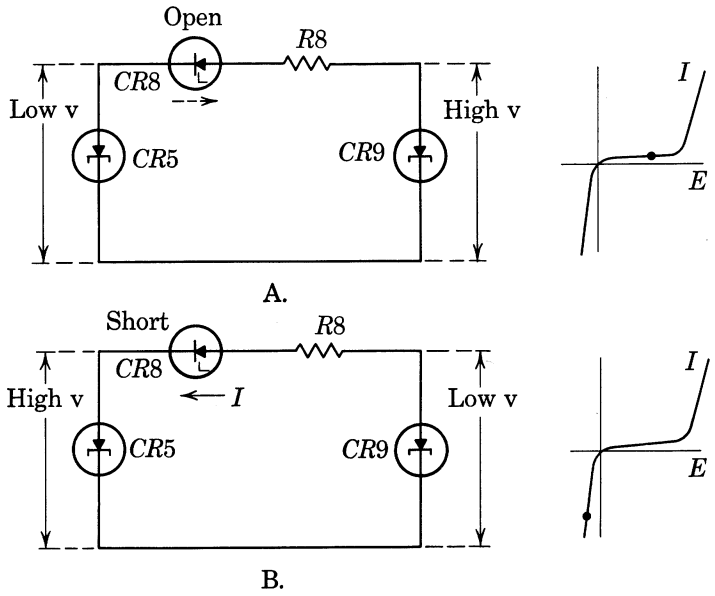


FIG. 8–16. Partial schematic, gate and output diodes, showing effect of different voltage states on backward diode

because the diodes are back-to-back. Similarly backward diodes *CR*6, *CR*7, and *CR*8 prevent interaction between any of the output circuits.

Note: Throughout this text the arrowhead on the graphical symbol for any crystal diode represents *p*-type semiconductor material. In some technical literature the arrowhead represents *p*-type material for tunnel diodes and normal rectifying diodes, but then represents *n*-type material for the backward diode.

8–15. AND or OR Gate, Circuit Analysis

If the basic bistable circuit shown in dashed lines in Fig. 8–13 is biased as indicated in Fig. 8–11B the circuit can be operated as an AND gate (*a* below). If biased as indicated in Fig. 8–11C, the circuit can be operated as an OR gate (*b* below). A discussion of the function of all the parts in the circuit is given in paragraph 8–14.

a. AND Gate. Under quiescent conditions diode *CR*5 (Fig. 8–13) is biased at a low current point in the *on* region. When *all* the preceding tunnel diode stages switch to the *off* state, diode *CR*5 receives sufficient current to exceed its peak current and switches rapidly to the *off* state. In turn the resultant high voltage across diode *CR*5 switches each succeeding stage that is in the *on* state to the *off state.*. To return diode *CR*5 to the *on* state a negative reset pulse is normally introduced at the diode anode. To assure proper operation as an AND gate, several conditions must be met. (Note that in the circuit each input current *adds* to diode *CR*5 current because resistor *R*5 and battery E_B act as a constant-current source that delivers a current I_B at all times. Likewise each output current subtracts from diode *CR*5 current for the same reason.)

1. The sum of the maximum bias current (I_B) plus the maximum values of any two of the input currents (I_1, I_2, or I_3) must be less than the minimum value of the diode *CR*5 peak current (I_p); otherwise the diode will switch with less than *all* inputs present. The terms maximum and minimum are used here, because the indicated current will vary with temperature; in addition they depend on the tolerances of the circuit elements.

2. The sum of the minimum values of all the input currents plus the minimum value of the bias current must be larger than the maximum value of the diode *CR*5 peak current; otherwise the circuit will not switch even when all inputs are present.

3. The minimum value of bias current (I_B) *less* the maximum value of all output currents (I_4, I_5, and I_6) must be greater than the maximum value of the diode *CR*5 valley current (I_v); otherwise the circuit will switch to the *on* state before application of a reset pulse. In practice this condition is usually very difficult to meet with the given circuit. The reason is the

very low value of bias current (I_B) required for AND gate operation. This in turn would require extremely low values of output current. An improved version of this circuit, known as Chow's circuit, is discussed in paragraph 8–16.

b. OR Gate. Under quiescent conditions diode $CR5$ is biased at a high current point in the *on* region. When any one of the preceding tunnel diode stages switch to the *off* state, diode $CR5$ receives sufficient current to exceed its peak current and switches rapidly to the *off* state. In turn, succeeding stages in the *on* state are switched to the *off* state. To assure operation as an OR gate, several conditions must be met:

1. The maximum value of bias current (I_B) must be less than the minimum value of the diode $CR5$ peak current; otherwise the circuit will switch of its own accord to the *off* state.
2. The minimum value of bias current plus the minimum value of any one input current (I_1, I_2, or I_3) must be greater than the maximum value of the diode $CR5$ peak current; otherwise the circuit will not switch to the *off* state with *one* input pulse present.
3. The condition stated in *a*3 above for the AND gate also applies for the OR gate. The difficulty encountered for the practical AND gate, however, normally does not apply to the OR gate because in the latter case bias current (I_B) is much higher.

8–16. Chow's Circuit

The AND gate shown in Fig. 8–17 is named after the originator, W. F. Chow of the General Electric Company. Basically the circuit is similar to that shown in Fig. 8–13 and discussed in paragraphs 8–14 and 8–15. The main difference is the addition of a second tunnel diode ($CR4$) across the

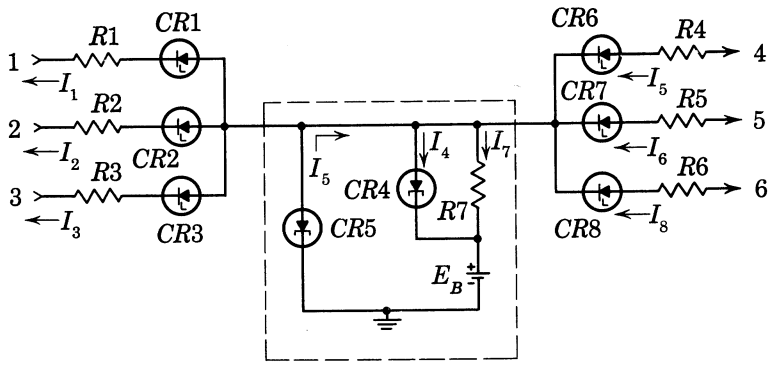


FIG. 8–17. Chow's circuit (Adapted circuit, courtesy General Electric Company)

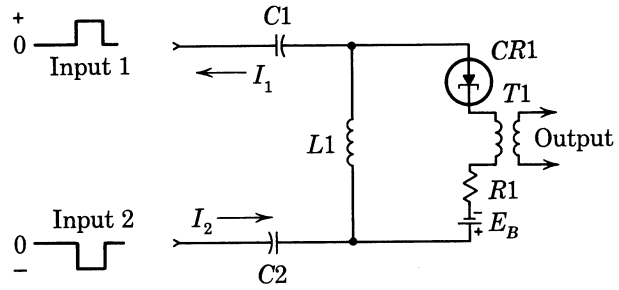
load resistor ($R7$) of the basic bistable circuit shown in dashed lines (Fig. 8–17). This second tunnel diode in turn eliminates the severe output condition experienced with the previous circuit (par. 8–15*a*3). The input and output resistors ($R1$ through $R6$) and the input and output backward diodes perform the same functions as those of the previous circuit.

a. In the previous circuit (Fig. 8–13) the bias current remained a fixed quantity whether diode $CR5$ was in the *on* or the *off* condition. For an AND circuit it is desired to have a low bias current when the diode is in the *on* state and a high bias current when the diode is in the *off* state. With fixed-bias current (constant-current source) only a limited compromise is possible; this condition limits the number of stages that can be fed by the AND gate. Otherwise the possibility of the current through the diode falling below its valley current is risked and unwanted switching occurs.

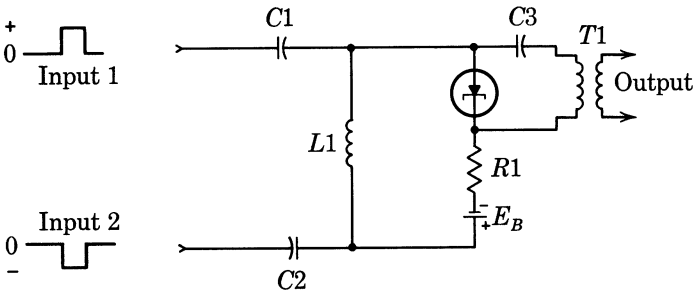
b. Chow's circuit (Fig. 8–17) permits a low bias current to be delivered by battery E_B when diode $CR5$ is in the *on* state, and a high bias current to be delivered by battery E_B when diode $CR5$ is in the *off* state. The voltage value of battery E_B is limited so that only one of the two tunnel diodes ($CR5$ or $CR4$) can be in the high-voltage state; i.e., $E_B = E_p + E_v$ of the diode. In the initial operating condition diode $CR5$ is in the *on* state and diode $CR4$ is in the *off* state. The latter diode draws its low valley current. The total current through diode $CR5$ equals the current through diode $CR4$ and the current through load resistor $R7$. The value of load resistor $R7$ therefore depends upon the number of input pulses. The value is chosen to draw high current for few inputs and very low current for more inputs. When diode $CR5$ is switched to the *off* state by the sum of the input pulses, diode $CR4$ must switch to the *on* state. In the *on* state diode $CR4$ resistance is low and a current almost equal to its peak current can be delivered by battery E_B, plus the current through resistor $R7$. Diode $CR4$ can be selected so that its peak current is much higher than that of diode $CR5$. The current now available for delivery to the following stages (ignoring the current through resistor $R7$) is the difference in diode $CR4$ peak current and diode $CR5$ valley current. To assure AND circuit operation the conditions stated in paragraph 8–15*a*1 and 2 must be met. In addition, the maximum valley current of diode $CR5$ plus the maximum value of all the output currents (I_4, I_5, and I_6) must be less than the minimum peak current of diode $CR4$. Otherwise the circuit will switch to the initial bias condition without application of a reset pulse if diode $CR4$ peak current is exceeded.

8–17. AND Gates, Separate Input Terminals

a. Input Pulses of Unlike Polarity. A variation of the basic AND gate is shown in Fig. 8–18A. The basic bistable circuit consists of diode $CR1$,



A. Output proportional to diode current change

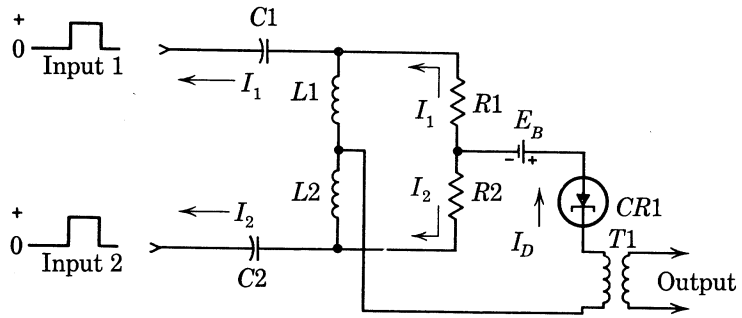


B. Output proportional to diode voltage change

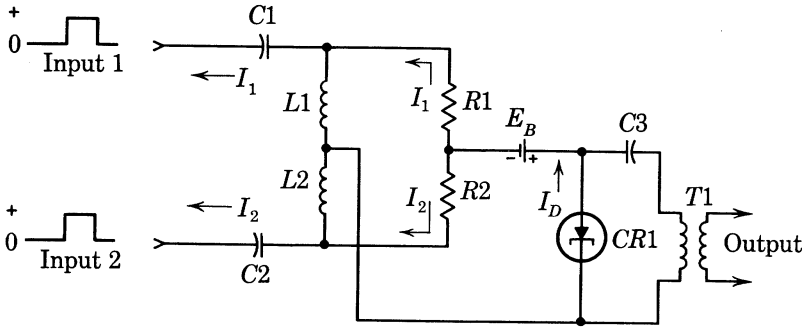
FIG. 8–18. AND gates with separate input terminals and requiring input pulses of unlike polarity

resistor $R1$, and bias battery E_B. The circuit is arranged so that an output will result with one positive input pulse and one negative input pulse. Essentially this condition is obtained by introducing the pulses at opposite ends of the diode. In addition to permitting the use of pulses of opposite polarity, the arrangement offers good isolation of the pulse sources from each other. Capacitors $C1$ and $C2$ are dc blocking capacitors and couple the input pulses to the circuit. Coil $L1$ offers a high ac impedance to the input pulses, and a low dc resistance to the diode bias current. The output is coupled to the following stage through step-up transformer $T1$. Because the diode current flows through the primary of transformer $T1$, the output signal is proportional to the diode current change. Figure 8–18B shows a circuit that is similar in all respects except that the output is proportional to the change in diode voltage. This is accomplished by placing the primary of transformer $T1$ in parallel with the diode through dc blocking capacitor $C3$. AND circuit operation is assured by limiting each input pulse voltage to slightly more than half of the total input voltage required to switch the diode from the *on* to the *off* state.

b. Input Pulses of Like Polarity. Another variation of the basic AND gate is shown in Fig. 8–19A. The basic bistable circuit consists of diode $CR1$, battery E_B, and resistors $R1$ and $R2$; the effective load line is equal to the parallel resistance value of resistors $R1$ and $R2$. Capacitors $C1$ and $C2$ are dc blocking capacitors. Coils $L1$ and $L2$ offer a high ac impedance to the input pulses and a low dc resistance to the diode bias current. The output of step-up transformer $T1$ is proportional to the diode current change. Two positive-going input pulses are required for switching. The pulses are actually fed to the diode anode through isolating parallel networks. Two negative-going input pulses could be used if the battery and diode are connected in opposite directions in the circuit. The circuit shown in Fig. 8–19B is identical in all respects except that step-up transformer $T1$ is in parallel with diode $CR1$ through dc blocking capacitor $C3$. The output therefore is proportional to the voltage change across the diode. AND gate operation is assured by limiting each input pulse current to slightly more



A. Output proportional to diode current change



B. Output proportional to diode voltage change

FIG. 8–19. AND gates with separate input terminals and requiring input pulses of like polarity

than half the total input current required to switch the diode from the *on* to the *off* state.

8–18. NOT Gate or EXCLUSIVE OR Gate

The circuit shown in Fig. 8–20 can be used as a NOT gate or an EXCLUSIVE OR gate. As a NOT gate (*a* below) it is required that the peak current of diode $CR1$ be relatively low. As an EXCLUSIVE OR gate (*b* below), it is required that the peak current of diode $CR1$ be relatively high. Either application is best analyzed by graphical means. Resistor $R1$ is the pulse-source isolating resistor if the circuit is used as a NOT gate. Resistors $R2$ and $R3$ are pulse-source isolating resistors if the circuit is used as an EXCLUSIVE OR gate. Bias battery E_B and resistor $R4$ form a constant-current source that delivers a fixed current (I_B). Diode $CR1$ is considered the diode that is being switched, whereas diode $CR2$ and resistor R_L, in series, are considered to form a *load* for diode $CR1$. The output is taken across resistor R_L. The effective *load* formed by diode $CR2$ and resistor R_L is obtained by considering the graphs shown in Fig. 8–21. Refer to Fig. 8–20 for the current and voltage designations used. In Fig. 8–21A the current through and the voltage across diode $CR2$ (I_2 vs E_2) is

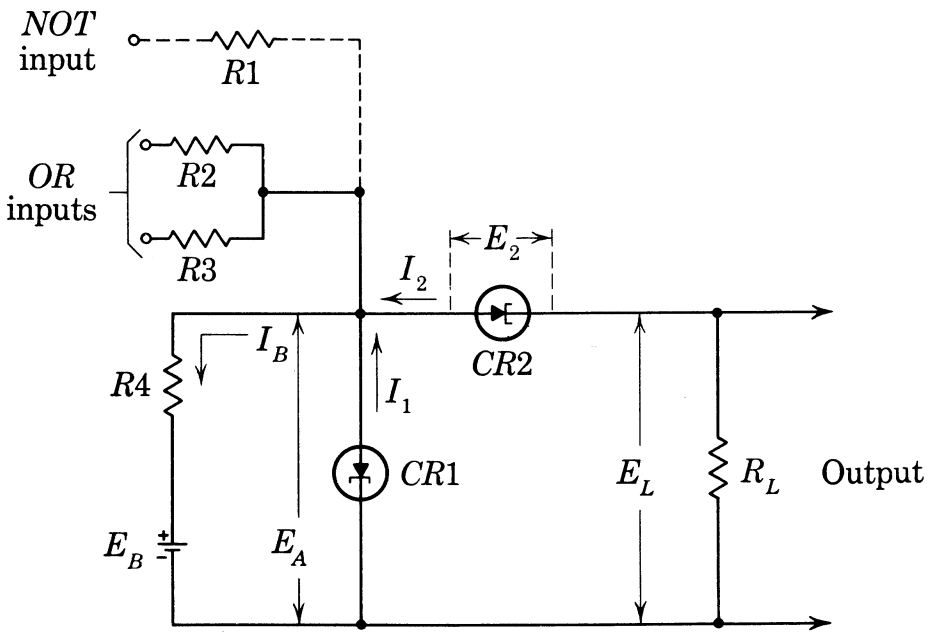


FIG. 8–20. NOT gate or EXCLUSIVE OR gate

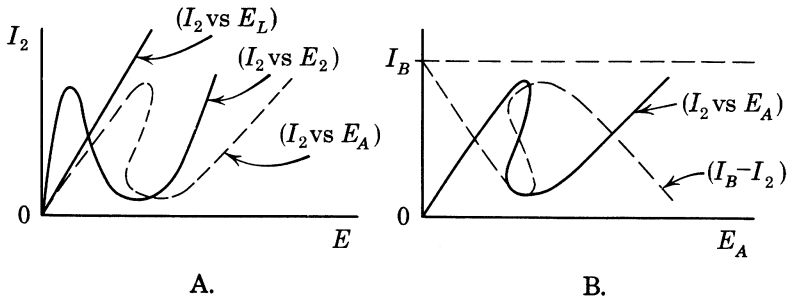


FIG. 8–21. Development of an effective parallel load line formed by a tunnel diode and a resistor

drawn; the current through and the voltage across resistor R_L (I_2 vs E_L) is drawn. Note that the current through diode $CR2$ and resistor R_L is the same and that the applied voltage (E_A) equals the sum of the voltages across these two elements ($E_A = E_2 + E_L$). If diode and resistor curves are added point for point in a horizontal direction, their composite curve (I_2 vs E_A) is obtained. In Fig. 8–21B the composite curve (I_2 vs E_A) is subtracted from the fixed bias current (I_B) and the difference ($I_B - I_2$) represents the effective load. Actually $I_B - I_2$ equals I_1. When the curve ($I_B - I_2$) is superimposed on diode $CR1$ current-voltage curve, the points of intersection in the positive-resistance regions will be the stable operating points; i.e., those points are the only points that represent a *compatible* division of bias current between the two branches of the circuit.

a. NOT Gate. Figure 8–22A shows diode $CR1$ curve (I_1) and the effective load ($I_B - I_2$) formed by diode $CR2$ and resistor R_L. Note that diode $CR1$ has a low peak current. Points 1 and 2, both in the high-voltage region of diode $CR1$, are the only stable points. When the power is first turned on, the circuit stabilizes at point 1. Here the current through diode $CR1$ is low;

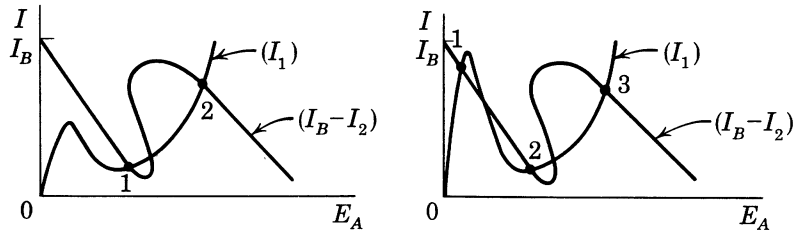


FIG. 8–22. Biasing relationships for NOT gate and EXCLUSIVE OR gate

that through resistor R_L is high and the output voltage is a high positive value. A positive input current switches the circuit to point 2. Here the current through diode $CR1$ is high; that through resistor R_L is low and the output voltage is low. A negative input current now has the opposite effect. The circuit therefore performs the NOT or inversion function.

b. EXCLUSIVE OR Gate. Figure 8–22B shows diode $CR1$ curve and the effective load $(I_B - I_2)$. Note that in this case diode $CR1$ has a high peak current which results in *three* stable operating points. At point 1 the current through resistor R_L is low and the output voltage is low. If *either* input pulse of high magnitude is present, the circuit will switch to point 2 which is a high-voltage output point. If *both* input pulses of high magnitude are present, the circuit will switch to point 3 which is a low-voltage output point. The EXCLUSIVE feature refers to whether the output will be a high- or a low-voltage output.

8–19. MAJORITY Gate, Goto Pair

The MAJORITY gate shown in Fig. 8–23A is named after the originator, E. Goto of the University of Tokyo. Basically the circuit consists of the coupled-pair or twin-diode arrangement, the current-voltage characteristic of which is discussed in detail in paragraph 6–7. The supply voltage $(2E_s)$, however, consists of a pulse coupled into the circuit through transformer $T1$. During operation the supply voltage pulse is rising when the trigger input pulses are introduced. The input pulses are coupled through isolating resistors R_s. The outputs are taken through isolating resistors R_s. These resistors (considered to be all in parallel and of equal value) also form a bistable load line with the current-voltage characteristic of terminals 2–2′ (Fig. 8–23B). The circuit is stable at points 1 and 2. Note that an odd number of inputs are used. Both negative and positive input trigger pulses are used. If the sum of the input currents causes a net electron flow (I_{in}) into terminal 2′, the circuit will stabilize at point 2 and the output voltage will be positive with respect to ground. If the sum of the input currents causes a net electron flow (I_{in}) out of terminal 2′, the circuit will stabilize at point 1 and the output voltage will be negative. In other words, the polarity of the output voltage depends upon the polarity of the majority of the input pulses. The circuit is reset each time the supply voltage pulse drops to zero.

Note: The Goto pair is actually one example of tunnel diode *locking* circuits. Locking circuits usually do not have a dc power supply and are receptive to input signals only during the time that the power supply waveform rises from zero to its maximum value. The circuit then *locks* into one of its two possible stable states. Another example of a locked pair is discussed in paragraph 8–20.

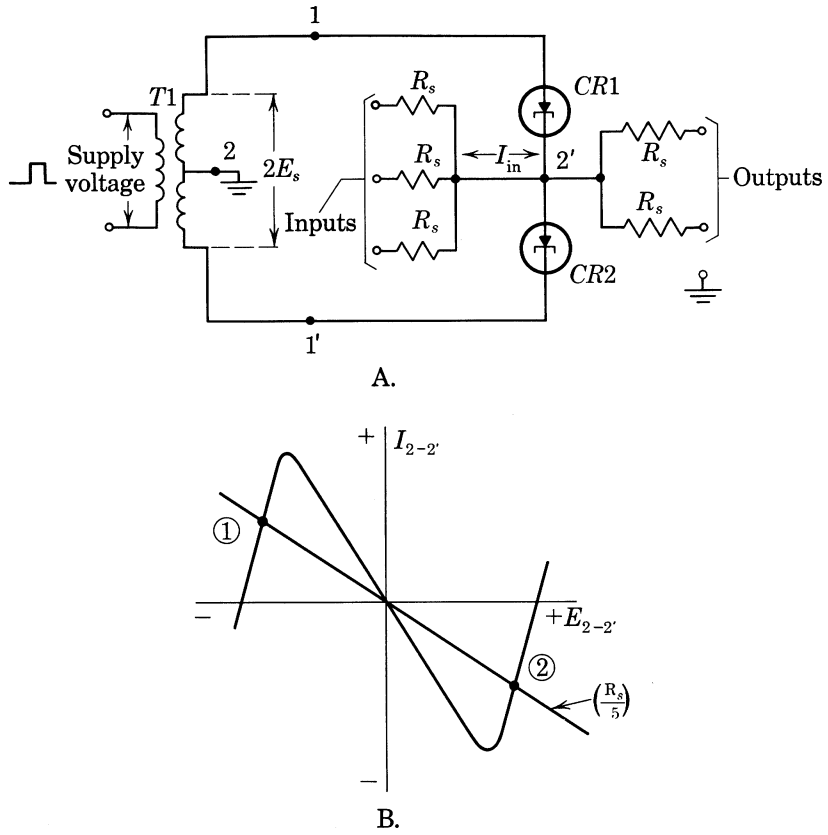


FIG. 8–23. Goto pair MAJORITY gate, and bistable arrangement of characteristics

8–20. Majority Gate, Single-Ended Locked Pair

a. Like the Goto pair (par. 8–19), the circuit shown in Fig. 8–24 is classified as a locking circuit; the input power is in the form of a rectangular pulse coupled into the circuit by transformer $T1$. Unlike the Goto pair, the output is taken from anode to cathode of one tunnel diode and is therefore a *single-ended* circuit. The secondary of the input transformer need not be center-tapped. In this circuit, the two diodes are matched. Resistors $R1$, $R2$, and $R3$ are the input isolating resistors. Supply voltage E_s is limited so that only one of the two diodes can be in the *off* state. The circuit therefore is stable with diode $CR1$ in the *off* state and diode $CR2$ in the *on* state, or vice versa.

b. Pulses of mixed polarity are introduced into terminals 1, 2, and 3 at

the same time that the power supply pulse is rising in magnitude. Current I_1 in diode $CR1$ and I_2 in diode $CR2$ start to rise.

1. If negative input pulses predominate, input current I_{in} flows *toward* the junction of the diodes; this current adds to current I_1 and causes diode $CR1$ to exceed is peak current and switch rapidly to its *off* state. Diode $CR1$ remains in the *on* state and the output voltage is low.
2. If positive input pulses predominate, input current I_{in} flows *away* from the junction of the diodes. This current adds to current I_2 and causes diode $CR2$ to exceed its peak current and switch rapidly to its *off* state. The output voltage is high.
3. Thus the magnitude of the output voltage depends upon the polarity of the *majority* of the input pulses.

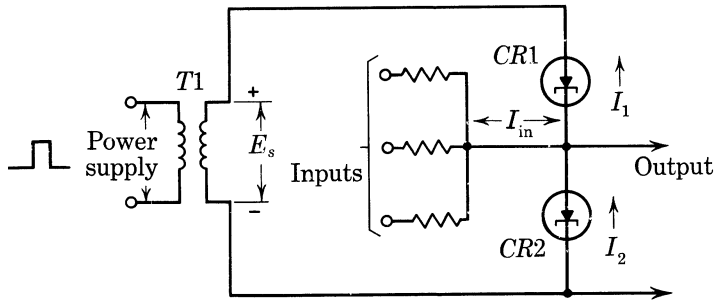


FIG. 8–24. Single-ended, locked pair MAJORITY gate

8–21. AND or OR Locking Circuit

The locking circuit shown in Fig. 8–24 can also be designed for use as an AND gate or an OR gate. This can be accomplished by using two tunnel diodes having different peak currents. As an AND gate (*a* below) the difference in peak currents must be relatively large. As an OR gate (*b* below) the difference in peak currents must be relatively small. The power supply limitations are the same as for the MAJORITY gate (par. 8–20).

a. AND Gate. Assume that the diode $CR1$ has a much lower peak current than diode $CR2$. With no input pulses except from the power supply, diode $CR1$ will always reach its peak current first and switch to the *off* state. Diode $CR2$ must remain in the *on* state and the output voltage is low. If all the input pulses of predetermined value are present and positive-going (drawing current from the junction of the diodes) when power is turned on, the aiding effect on diode $CR2$ will cause it to switch to the *off* state first. The output voltage is high. AND circuit operation is assured by having the difference in the diode peak currents sufficiently large that *all* inputs must be present to cause diode $CR2$ to switch first. All negative-going input pulses can also be used. In this case diode $CR1$ will have a *higher* peak current than diode $CR2$. When all input pulses are present, the output voltage will be low instead of high as with positive-going input pulses.

b. OR Gate. The operation of the locking circuit as an OR gate is identical with its operation as an AND gate (*a* above). The peak currents of the diodes, however, are only slightly different in magnitude, and effective switching can be accomplished with only one input pulse present.

8–22. Summary

a. Switching circuits perform triggering, gating, inverting, and signal routing functions.

b. Pulse and switching circuits are characterized by large-signal operation.

c. A unit-step voltage (or current) refers to an instantaneous change in amplitude either positive- or negative-going.

d. When biased in the low-voltage state, the tunnel diode is considered to be *on;* in the high-voltage state, it is *off*.

e. The basic monostable multivibrator requires a bias voltage, a load resistor, a tunnel diode, and an energy-storing element, such as a coil. The monostable multivibrator may be stable in the *on* region or the *off* region.

f. The basic bistable multivibrator requires a bias voltage, a load resistor, and a tunnel diode. The bistable multivibrator is stable in the *on* region and the *off* region.

g. The basic bistable multivibrator can be made more sensitive by shunting the tunnel diode with a normal rectifying diode in series with a low-valued resistor (par. 8–7). The resultant output waveform has almost equal dwell periods. The base-emitter junction of a transistor can be substituted for the rectifying diode.

h. Monostable or bistable multivibrators can be constructed from a coupled pair. Trigger pulses of the *same* polarity can be used for switching in either direction (par. 8–8).

i. A controlled-negative-resistance multivibrator (par. 8–9) produces a variable-amplitude output waveform.

j. By using a multistate switch composed of several tunnel diodes in series, a pulse-frequency divider and staircase generator can be formed (par. 8–10).

k. Most AND or OR gates are similar except for the bias points used in the basic bistable circuit.

l. Inversion of the output of an AND or OR gate results in a NOT AND or NOR gate, respectively.

m. Unidirectional flow of energy (or information) is achieved in certain gating circuits (par. 8–14) by using backward diodes at the input and output terminals.

n. A backward diode may be considered a *low-voltage* rectifying diode.

o. A NOT gate can be formed by using a tunnel diode and a series resistor combination as a parallel load for the *active* tunnel diode (par. 8–18).

p. The EXCLUSIVE OR gate uses similar components as the NOT gate (*o* above). The NOT gate has two stable operating points; the EXCLUSIVE OR gate has *three* stable operating points.

q. A locking circuit is one that is receptive to input pulses only during the rising portion of the power supply waveform.

r. The Goto pair MAJORITY gate is a special application of the coupled pair in a locking circuit.

s. By using two tunnel diodes in a single-ended locking circuit (par. 8–20 and 8–21), a MAJORITY gate, and AND gate, or an OR gate can be formed.

Chapter 9

MODULATORS, DEMODULATORS, AND HETERODYNE DETECTORS

SECTION I. MODULATORS

9–1. Modulation, General

The process of varying a particular characteristic of radio signal (a carrier) in accordance with the amplitude of a signal that represents intelligence, such as speech or music, is called *modulation.* The most commonly used types of modulation are called amplitude modulation (AM) and frequency modulation (FM); these processes are discussed briefly in paragraphs 9–2 and 9–5, respectively.

9–2. Amplitude Modulation

The basic process of amplitude modulation (AM) is represented in block form in Fig. 9–1. The amplitude of a *carrier* (RF signal) is varied in accordance with the amplitude of a *modulating signal.* The latter signal, usually of low frequency (20 cps to 20 kc), is an electrical representation of the intelligence to be transmitted. The most direct method of producing an amplitude-modulated carrier uses the technique of varying the gain of

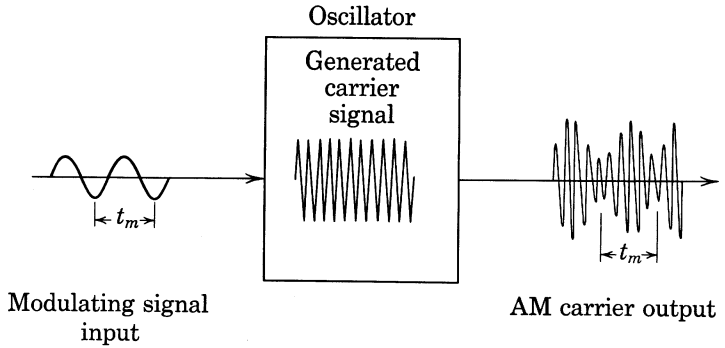


FIG. 9–1. Block diagram of amplitude-modulated oscillator